# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*In re* Patent Application of:

William D. Corti

Serial No.: 09/683,091

Confirmation No.: 8058

Filed: November 16, 2001

For: ON-CHIP LOGIC ANALYZER

Docket No.: BUR9200000199

Group Art Unit: 2184

Examiner: Wilson, Yolanda L.



Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## DECLARATION UNDER 37 C.F.R. § 1.131

Sir:

We, Steven C. Parker, Joseph O. Marsh, Robert Kenny, Jr., Michael Won, William D. Corti and Frank X. Scanzano, do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1, 17, and 19 of the above-identified application.

2. We completed the invention of claims 1, 17 and 19 (and those claims dependent thereon) in the United States before October 1, 1999, as evidenced below.

### CONCEPTION

3. Before October 1, 1999, we conceived of an on-chip logic analysis system including a single chip device including a signal processing unit and a host unit externally provided as disclosed and recited in independent claims 1, 17 and 19 of the application, of which is evidenced by notebook documentation attached hereto as Exhibit A. The notebook documentation attached hereto is a photocopy of and is identical to the originals, except that all pertinent dates have been removed therefrom.

4. All pertinent dates removed from the notebook documentation attached hereto are before October 1, 1999.

5. The information shown in the notebook documentation was used to complete an Invention Disclosure attached as Exhibit B.

6. As evidenced by the attachments the on-chip logic analysis (OCLA) system includes:

a. a single chip device (e.g., DSP core logic) including a signal processing unit, a plurality of memory blocks, and a data capturing unit;

b. a host unit externally provided to said single-chip device and generating control signals to control the data capturing unit; and

c. the data capturing unit captures data processed by the signal processing unit in response to the control signals from the host unit and transfers the captured data to the host without interrupting operations of the signal processing unit.

7. In further embodiments, as evidenced by the attachments, e.g., notebook documentation, the on-chip logic analysis system also includes, for example:

a. an OCLA unit capturing data processed by the signal processing unit in response to the control signals from the host unit and transfers the captured data to the host without interrupting operations of the signal processing unit; and

b. a DSP core logic.

8. The benefits and features of the on-chip logic analyzer are shown and described in the attachments.

9. These features and others are exemplified in the figures in at least the notebook documentation, all of which is a complete and permanent idea of the complete and operable invention.

DUE DILIGENCE

10. Prior to October 1, 1999, the inventors worked diligently on the invention as recited in the claimed invention, and the subsequent above-identified application until such application was completed on November 13, 2001.

11. During this time, we worked diligently in providing information to IBM in-house counsel in order to begin the preparation of a patent application for filing in the U.S. Patent Office. All of the inventors were involved in working diligently in providing IBM in house counsel the pertinent information relating to the inventive concept, including completing the attached Inventor Disclosure, much of which is incorporated from the notebook documentation. For example, the pertinent information was communicated to IBM in-house counsel on or before December 7, 1999.

12. Prior to the filing of the above-identified application in the U.S. Patent Office, Inventor Parker communicated with patent counsel at McGuireWoods LLP, on behalf of all of the inventors, in preparing such patent application based on the notebook documentation and the subsequently submitted Invention Disclosure. We worked diligently on the preparation of the patent application with patent counsel at McGuireWoods until a final draft patent application was completed to our satisfaction. All of the inventors were involved in reviewing and finalizing the application for the present invention prior to the filing of the above-identified application. For example, communications took place on July 9 and 19, 2001, August 23, 2001 and up to and including correspondences dated November 7, 2001.

13. A final draft of the application was forwarded to us by IBM in-house attorney, Richard Henkler, who received the final draft from then McGuireWoods' attorney Kevin Reif in a letter dated November 13, 2001. At all times, we worked diligently to finalize the application for filing in the U.S. Patent and Trademark Office from prior to October 1, 1999 to the finalized application on November 13, 2001, as evidenced herein.

14. The patent application was filed in the U.S. Patent and Trademark Office on November 16, 2001.

15. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may

jeopardize the validity of the application or any patent issuing thereon.

Steven C. Parker — Date 5/7/04

Joseph O. Marsh — Date 5/7/04

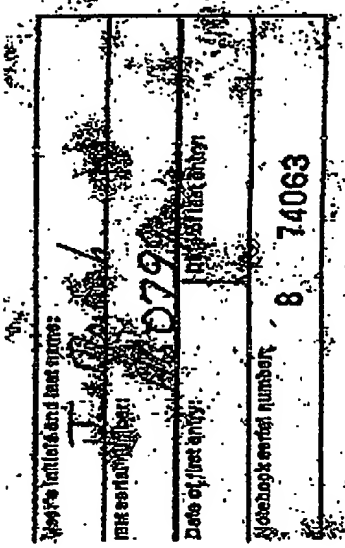
Robert Kenny, Jr. — Date 6/30/04

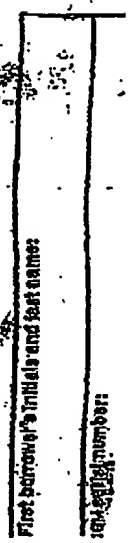
Michael Won — Date 5/12/04

William Corti — Date 5/12/04

Frank X. Scanzano — Date 5/18/04

WOOM\222253.2



8 74063 IBM Technical Notebook

- DSP - Internal Trace Buffer

10/22/97 - Concept: The internal SARAM will be partitioned into sectors & boundaries each at reset configuration will be detected and some portion of the SARAM (0 → #1.) may be configured as trace buffer.

1. From the JTAG port using Following IEEE Spec 1149.1 This memory could be configured read and written to.

2. Once configured ~~[redacted]~~ Trigger points can be scanned in to trigger on such events as Program Address, Program Data, Data Address, Data (Specific value), Read, write I/O or mem etc.

3. When the Configured Buffer is full an Interrupt at the JTAG port would signal (Buffer full signal) the debug Tool to scan the buffer from ~~[redacted]~~ Analysis. This would occur without stopping the processor allowing real Time processing of application to continue.

4. Other controls could be scanned into the JTAG port to give Commands to the test circuits & Halt, run step/step etc.)

The above understood and witnessed by [signature] Date [redacted] and by [redacted] Date [redacted]